Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-11. (Canceled).

12. (Currently Amended) A method ~~of communicating with a field programmable gate array (FPGA),~~ comprising:

establishing an interface between a host computer and ~~said FPGA~~ a general purpose programmable hardware device;

transmitting configuration information over said interface in a first transmission mode to configure the ~~FPGA~~ general purpose programmable hardware device to function according to a programmed configuration as virtual device under test; and

transmitting operation information from said virtual device under test emulating operation of an actual device under tests and operation information from said actual device under test over said interface in a second transmission mode.

13. (Currently Amended) The method according to claim 12, wherein the programmed configuration comprises operation as ~~a~~ the virtual device under test in an In-Circuit Emulation system.

14. (Original) The method according to claim 12, wherein the programmed configuration comprises operation as a virtual microcontroller in an In-Circuit Emulation system.

15. (Previously Presented) The method according to claim 12, wherein said interface comprises an IEEE 1284 compliant interface.

16. (Currently Amended) A method ~~of communicating with a field programmable gate array (FPGA),~~ comprising:

communicating ~~an interface~~ configuration information between a host computer and ~~said FPGA~~ a virtual device under test (DUT) to configure ~~said FPGA~~ the virtual DUT to ~~act as a virtual microcontroller~~ emulate a DUT;

executing ~~instruction~~ instructions in synchronization on ~~a microcontroller device~~ the DUT and ~~said~~ the virtual ~~microcontroller~~ DUT; and

transmitting operation information, from said executing by the DUT and the virtual DUT, between ~~said~~ the host computer and ~~said FPGA using said interface~~ the virtual DUT.

17. (Currently Amended) The method according to claim 16, wherein ~~said~~ an interface for said communication and said transmitting comprises an IEEE 1284 compliant interface.

18. (Currently Amended) The method according to claim 16, wherein ~~said FPGA~~ the virtual DUT is further configured to incorporate said interface.

19. (Currently Amended) A method ~~of communicating with a field programmable gate array (FPGA),~~ comprising:

connecting a host computer to ~~the FPGA~~ a base station using a communication interface, wherein the base station includes a field programmable gate array (FPGA);

programming ~~a~~ an emulator configuration into the FPGA~~, the configuration incorporating an implementation of the communication interface~~ using the communication interface; and

~~carrying out non-programming communication between the host computer and the FPGA~~ receiving operation information from a device under test (DUT) and the FPGA emulating the DUT using the communication interface.

20. (Original) The method according to claim 19, wherein the communication interface comprises an IEEE 1284 compliant interface.

21. (Currently Amended) The method according to claim 19, where the emulator configuration further incorporating a virtual microcontroller.

22. (Currently Amended) The method according to claim 21, wherein the virtual microcontroller executes instructions in synchronization with ~~a microcontroller~~ the DUT to carry out In-Circuit Emulation functions.

23. (Currently Amended) A method ~~of communicating with an FPGA,~~ comprising:

transmitting interface information over a parallel communication interface of ~~an~~ a field programmable gate array (FPGA) ~~FPGA~~ to configure the FPGA to act as a parallel port;

transmitting emulator information to the FPGA ~~to receive data from a host computer system and~~ to configure the FPGA to operate as a virtual microcontroller in lock step with a microcontroller under test using the parallel port of the FPGA; and

receiving ~~data and communicating control~~ operation information, ~~at~~ generated by the virtual microcontroller and the microcontroller under test operating in lock step, from ~~said~~ the parallel port of ~~said~~ the FPGA~~, the virtual microcontroller operating in lock step with a microcontroller under test; and~~

~~commanding the FPGA with instructions from the host computer system using the communication interface that configured the FPGA~~.

24. (Original) the method according to claim 23, wherein the parallel port comprises an IEEE 1284 compliant parallel port.

25. (Original) The method according to claim 23, wherein bidirection IEEE 1284 compliant communication is carried out using extended parallel port (EPP) mode communication over the parallel port.

26. (Original) The method according to claim 23, further comprising conducting In-Circuit Emulation functions using the parallel port.

27. (New) The method according to claim 16, wherein the virtual DUT comprises a general purpose programmable device.

28. (New) The method according to claim 27, where the general purpose programmable device comprises a field programmable gate array.

29. (New) The method according to claim 19, wherein the DUT comprises a microcontroller.